REMARKS

Claims 1-13 have been examined, with all claims rejected. New claims 14-16 have been added.

Claim Rejections - 35 USC 112

Claims 1-13 have been rejected under 35 USC 112, second paragraph, as being indefinite. Applicant respectfully traverses this rejection for the reasons set forth below.

Regarding claim 1, it is clear from reading the claim in light of the specification that "real time aspects" of each application concern how much processing time is required by the application, how much processing time is available to the application, and what the latest time is for the application to finish the required processing.

Regarding claim 2, it is clear from reading the claim in light of the specification that "profiling" is performed in order to extract sufficient information for selecting desired time slice granularity. Examples of such information include the real time requirements described in the previous paragraph, overhead for context switch, algorithm complexity, memory requirements, etc. Profiling may be carried out by engineers, by computer programs, by other devices, or by a combination of all the above.

Regarding claim 6, it is clear from reading the claim in light of the specification that the "extracting" task delivers a set of information concerning requirements on what source data, intermediate data, result data, and application state information need to be stored and recovered for time slice based processing. This set of information, in turn, can be translated into a size of a data cache.

Regarding claim 13, it is clear from reading the claim in light of the specification that in the time-sliced processor, the "master controller unit" controls the operation of the other modules

including the "data cache" and the "plurality of finger processing elements" according to its "time slot table" and "partial sums search table".

In view of the above, it is respectfully submitted that the claims are definite. Reconsideration and withdrawal of this rejection is therefore respectfully requested.

Claim Rejections - 35 USC 103

Claims 1-13 have been rejected under 35 USC 103(a) as being unpatentable over Belotserkovsky et al. (U.S. Patent No. 6,621,857) in view of Schuster et al. (U.S. Patent No. 6,591,355). Applicant respectfully traverses this rejection for the reasons set forth below.

Claims 1-12

Independent claim 1 is directed to a method for building a time-sliced architecture in a spread spectrum system. First a set of applications is analyzed, and then a specific time-sliced architecture is built to accommodate the range of applications based on the analyzing. The analyzing includes extracting real time aspects from each application in the set of applications, determining an optimal granularity based on the real time aspects, and adjusting the optimal granularity based on a context switching overhead. Independent claim 7 corresponds to claim 1 in that it is directed to a computer program including logic code for performing the method of claim 1.

Belotserkovsky describes a spread spectrum transceiver system for TDMA (Time Division Multiple Access), which a communication protocol for data stream transmission of multiple users over a shared media. This protocol divides the available time into multiple time slots and dedicates one or more time slots to an individual user, or to more than one user if another multiplexing method is also used (e.g., Frequency Division, Frequency Hopping, and Direct Sequence Spreading). Nevertheless, for each TDMA user, only its dedicated time slot is valid for communication, and the time slot assignment for each user is usually periodic. A TDMA transceiver must be designed to be on for its assigned time slots and off for other time slots during the course of communication. Belotserkovsky's "time sliced" architecture is an obvious design

choice for a TDMA transceiver in order to process the time-slot-based user data packets. The processing granularity for Belotserkovsky's architecture is obviously a TDMA time slot, and there is no reason to adjust the processing granularity even if the granularity adjustment method were well known.

On the other hand, the claimed invention describes a method and apparatus for time sliced based communication signal processing scheme which is independent of the communication protocol. For example, in the exemplary embodiment presented in the application, CDMA (Code Division Multiple Access) is a communication protocol for data stream transmission from multiple users over a shared media by assigning each user a unique scrambling/channelization code and allowing all admitted users to transmit at all times (as opposed to during assigned time slots); a CDMA transceiver is on during the entire course of communication. In fact, any interruption to the operation of a CDMA transceiver during the course of communication is not desirable since that may result in loss of chip rate synchronization. Contrary to the common believe and practice, the method described in the patent application divides the signal processing operation of a CDMA transceiver in to time slices and only processes the signal for a particular CDMA transceiver on its dedicated time slices. Furthermore, the method described in the patent application supports dividing the signal processing operation during one time slot of a TDMA transceiver to multiple smaller time slices and only processes the signal for a particular TDMA transceiver in its dedicated time slices. It would not have been obvious to a person of ordinary skill to derive the time sliced signal processing method described in the patent application from a conventional TDMA transceiver such as the one described in Belotserkovsky.

Although the term "time slice" is used in both the patent application and Belotserkovsky, the term has different definitions in the two documents. In Belotserkovsky, "time slice" is a time slot in a TDMA system (see col. 4, line 43). In the patent application, on the other hand, "time slice" is the selected processing time granularity for performing time slice based transceiver signal processing; the term is not at all related to the time slot of a TDMA system.

Schuster describes a method for supporting distributed shared memory access in finer granularity than virtual page for multiple applications. Schuster teaches that the granularity adjustment is determined by the running applications according to their success rate in accessing the shared memory (col. 4, lines 53-67). It is obvious that the method is designed for adjusting paging granularity for distributed shared memory access in order to achieve improved efficiency, and not for adjusting processing time allocated in each processor for the applications. To one of ordinary skill, a method for memory access is not obviously applicable to processing time allocation and scheduling since it is well known that these systems involve two different types of design issues.

The method described in the patent application uses the concept of time slice based processing to allocate processing time for applications at desired time slice granularity. To select the appropriate time slice granularity, both the real time aspects of each application and context switch overhead are considered. The "real time aspect" of each application concerns how much processing time is required by the application, how much processing time is available to the application, and what the latest time is for the application to finish the required processing.

In addition, the claims are directed to "building a time-sliced architecture". Thus, the time slice granularity is selected before the applications are running in order to design and implement the time-sliced processor. Belotserkovsky is directed to a system that is already designed and built, and Schuster's method for adjusting the granularity for distributed memory access is only valid while applications are running (col. 4, lines 53-67).

Claims 1-12 are therefore patentable over the applied references for at least these reasons.

Claim 13

Independent claim 13 is directed to a time-sliced processor for use in a spread spectrum system. The processor includes a master control unit (110), a data cache (102) for receiving input data and for caching intermediate data, and a plurality of finger processing elements (104, 106, 108). The master control unit includes a time slot table (112) and a partial sums search table (112).

Each of the finger processing elements includes a cache (122) for receiving data from the data cache and for caching intermediate data, a data selector (124) connected to an output of the cache, a despreader (126) connected to an output of the data selector, and a symbol integrator (128) connected to an output of the despreader. See Figure 1.

A time slice based signal processing method requires that the signal processing for a particular transceiver is carried out only during its assigned time slice. If the complete processing operation requires more than one time slice, a time sliced processor needs to store sufficient processor date (i.e., state information and intermediate results) at the end of a time slice in order to continue the unfinished processing at the beginning of the next assigned time slice. While a complete processing operation is performed in multiple time slices, it is further required that the final results are identical to the ones that are obtained when the processing operation is carried out continuously from start to complete. It is also well known that maintaining chip rate synchronization is critical to the correct operation of spread spectrum systems, and a spread spectrum transceiver must be designed to maintain such synchronization irrespective of what architecture is used. The claimed time-sliced processor was designed specifically to fulfill the above requirements. The size of a time slice is independent of communication protocols and is a parameter available for optimizing other design criteria, such as power consumption, silicon area, etc.

On the other hand, Belotserkovsky's TDMA transceiver operates on TDMA time slot basis. To a person having ordinary skill in the art, it is understood that a complete processing operation of a TDMA slot is from the beginning of the slot to the end of the same time slot. Belotserkovsky's TDMA transceiver starts its operation at the beginning of its assigned TDMA time slot and continues to finish the operation at the end of the same time slot. As a result, it would not be reasonable for such a transceiver to include any modules or components or mechanisms for storing and recovering intermediate results and state according to the requirements for a time-sliced processor as described in the previous paragraph. Additionally, the size of a time slot in Belotserkovsky is a design specification dictated by the communication protocol.

The architecture according to Schuster is designed for adjust the granularity for shared memory access. It is obvious that such architecture is not suitable for adjusting processing time allocation as required by a time-sliced based signal processing method since they are two different design issues.

Claims 13 is therefore patentable over the applied references for at least these reasons.

Thus, it is respectfully submitted that the pending application is in condition for allowance.

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Respectfully submitted,

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